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Relevance scale ☐ ☐ ☐ ☐ ☐**1 [Register allocation with instruction scheduling](#)**

Shlomit S. Pinter

 June 1993 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1993 conference on Programming language design and implementation**, Volume 28 Issue 6
Full text available: [pdf\(931.91 KB\)](#)
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We present a new framework in which considerations of both register allocation and instruction scheduling can be applied uniformly and simultaneously. In this framework an optimal coloring of a graph, called the parallel interference graph, provides an optimal register allocation and preserves the property that no false dependences are introduced, thus all the options for parallelism are kept for the scheduler to handle. For this framework we provide heuristics for trading ...

2 [Optimum modulo schedules for minimum register requirements](#)

Alexandre E. Eichenberger, Edward S. Davidson, Santosh G. Abraham

 July 1995 **Proceedings of the 9th international conference on Supercomputing**
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3 [Global code motion/global value numbering](#)

Cliff Click

 June 1995 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1995 conference on Programming language design and implementation**, Volume 30 Issue 6
Full text available: [pdf\(1.13 MB\)](#)
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4 [Iterative modulo scheduling: an algorithm for software pipelining loops](#)

B. Ramakrishna Rau

 November 1994 **Proceedings of the 27th annual international symposium on Microarchitecture**
Full text available: [pdf\(1.49 MB\)](#)
 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Modulo scheduling is a framework within which a wide variety of algorithms and heuristics may be defined for software pipelining innermost loops. This paper presents a practical algorithm, iterative modulo scheduling, that is capable of dealing with realistic machine



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1 [Trace selection for compiling large C application programs to microcode](#)

P. P. Chang, W. W. Hwu

January 1988 **Proceedings of the 21st annual workshop on Microprogramming and microarchitecture**

Full text available:  [pdf\(833.92 KB\)](#)


Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Microcode optimization techniques such as code scheduling and resource allocation can benefit significantly by reducing uncertainties in program control flow. A trace selection algorithm with profiling information reduces the uncertainties in program control flow by identifying sequences of frequently invoked basic blocks as traces. These traces are treated as sequential codes for optimization purposes. Optimization based on traces is especially useful when the code size is large and the co ...

2 [An efficient resource-constrained global scheduling technique for superscalar and VLIW processors](#)

Soo-Mook Moon, Kemal Ebcioglu

December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture**, Volume 23 Issue 1-2

Full text available:  [pdf\(2.05 MB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: VLIW, compile-time parallelization, instruction-level parallelism, superscalar

3 [Parallelizing nonnumerical code with selective scheduling and software pipelining](#)

Soo-Mook Moon, Kemal Ebcioglu

November 1997 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 19 Issue 6

Full text available:  [pdf\(543.93 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Instruction-level parallelism (ILP) in nonnumerical code is regarded as scarce and hard to exploit due to its irregularity. In this article, we introduce a new code-scheduling technique for irregular ILP called "selective scheduling" which can be used as a component for superscalar and VLIW compilers. Selective scheduling can compute a wide set of independent operations across all execution paths based on renaming and forward-substitution and can compute availab ...